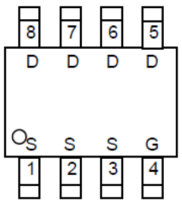
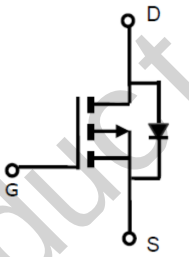
FEATURE

- ***-30V/-5.8A, $R_{DS(ON)}$=38mΩ (typ.)@V_{GS}=-10V***
- ***-30V/-4.0A, $R_{DS(ON)}$=60mΩ (typ.)@V_{GS}=-4.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOP8 package design



TOP VIEW
SOP-8



P-Channel

DESCRIPTION

The SI9435BDY-T1-E3 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

APPLICATIONS

- High Frequency Point-of-Load Synchronous
- Newworking DC-DC Power System
- Load Switch

ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current (T_A=25℃)	V_{GS}=10V	-5.8	A
	Continuous Drain Current (T_A=75℃)		-4.2	A
I_{DM}	Pulsed Drain Current		-20	A
I_S	Continuous Source Current (Diode Conduction)		-2.0	A
P_D	Power Dissipation	T_A=25℃	2.05	W
		T_A=70℃	1.5	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		85	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

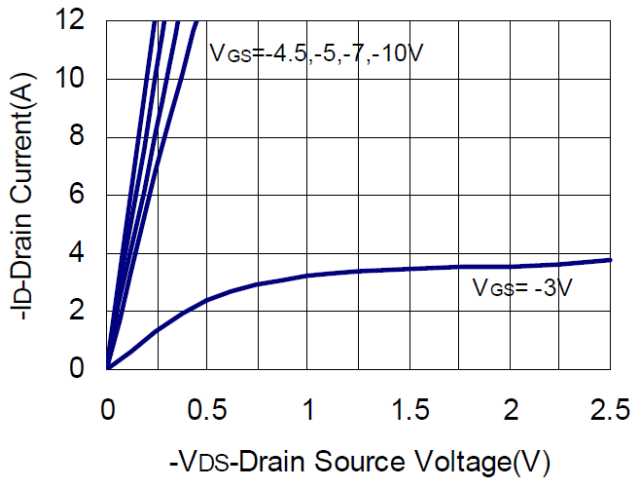
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.0		-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0			-1	uA
		V_{DS}=-24V, V_{GS}=0 T_J=55℃			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-10A		38	48	mΩ
		V_{GS}=-4.5V, I_D=-6.0A		60	78	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=-2.0A, V_{GS}=0V		-0.7	-1.2	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=-20V V_{GS}=-10V I_D=-5.8A		6.2		nC
Q_{gs}	Gate-Source Charge			2.5		
Q_{gd}	Gate-Drain Charge			3.3		
C_{iss}	Input Capacitance	V_{DS}=-15V V_{GS}=0V f=1MHz		640		pF
C_{oss}	Output Capacitance			270		
C_{rss}	Reverse Transfer Capacitance			103		
$T_{d(on)}$	Turn-On Time	V_{DS}=-15V I_D=-5A V_{GEN}=-10V R_G=3.3Ω		9.2		nS
T_r				16.5		
$T_{d(off)}$	Turn-Off Time			21.3		
T_f				21.5		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

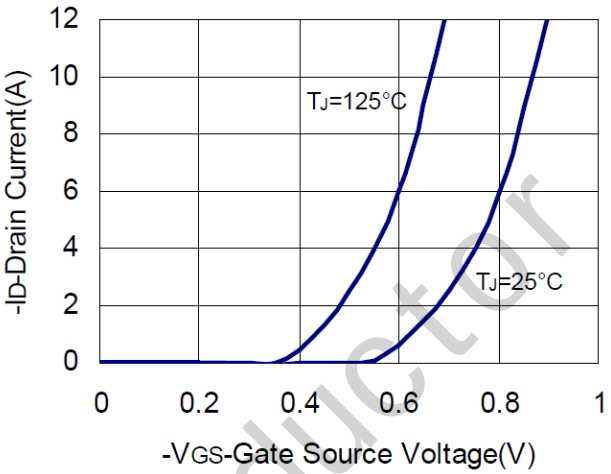
2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

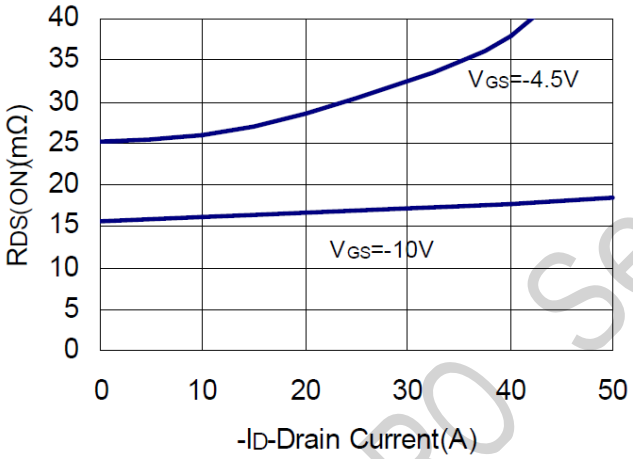
Output Characteristics



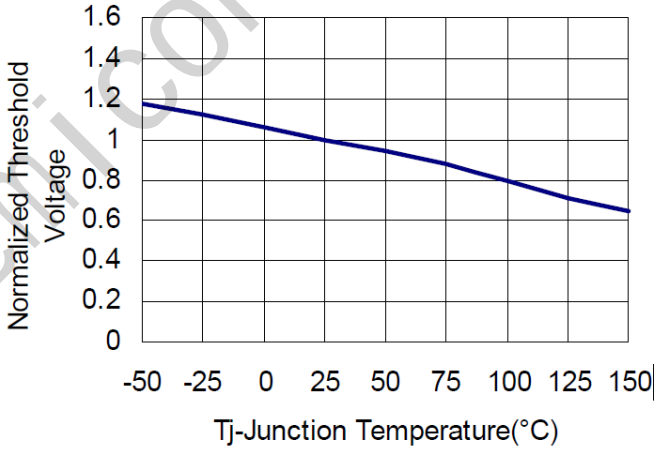
Transfer Characteristics



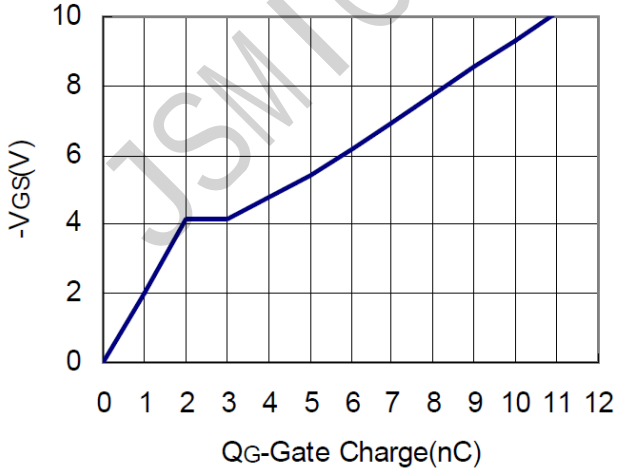
Drain Source On Resistance



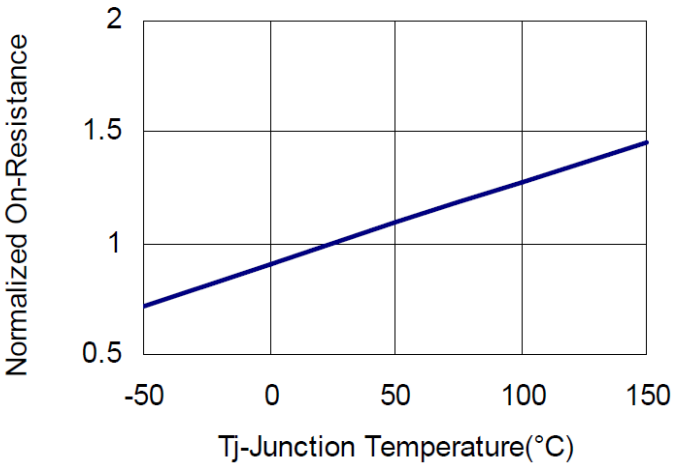
Gate Threshold Voltage



Gate Charge

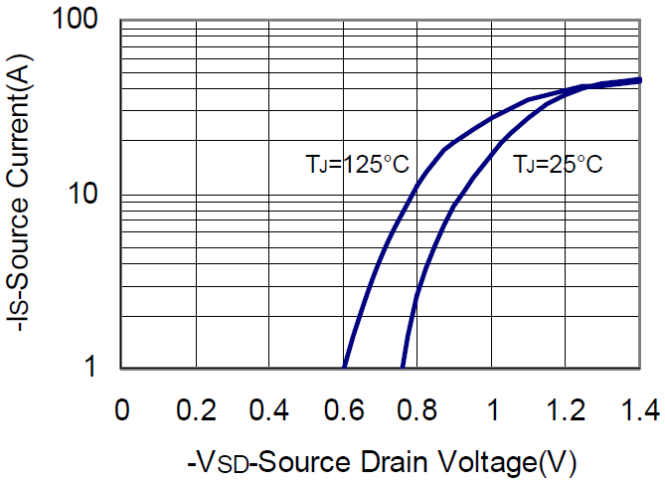


Drain Source Resistance

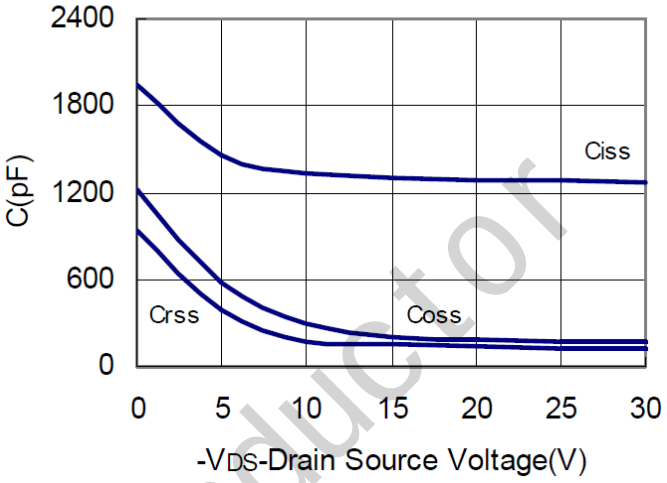


■ *TYPICAL CHARACTERISTICS (continuous)*

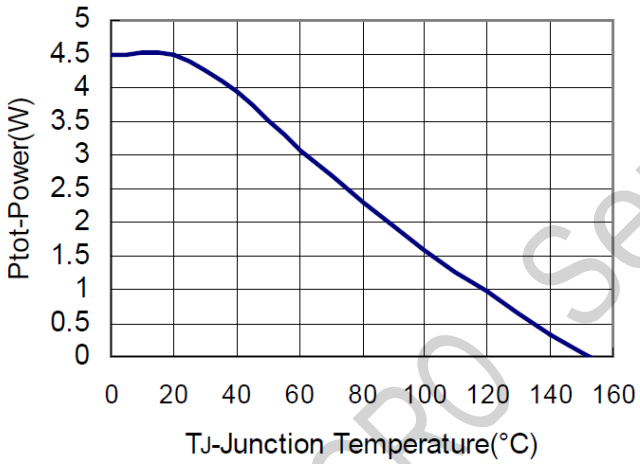
Source Drain Diode Forward



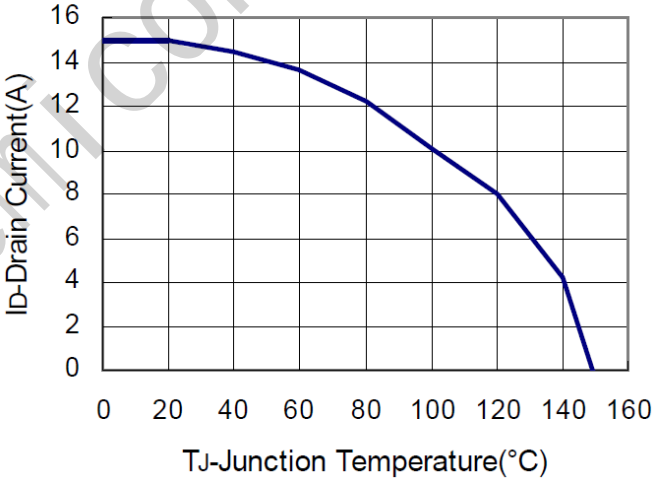
Capacitance



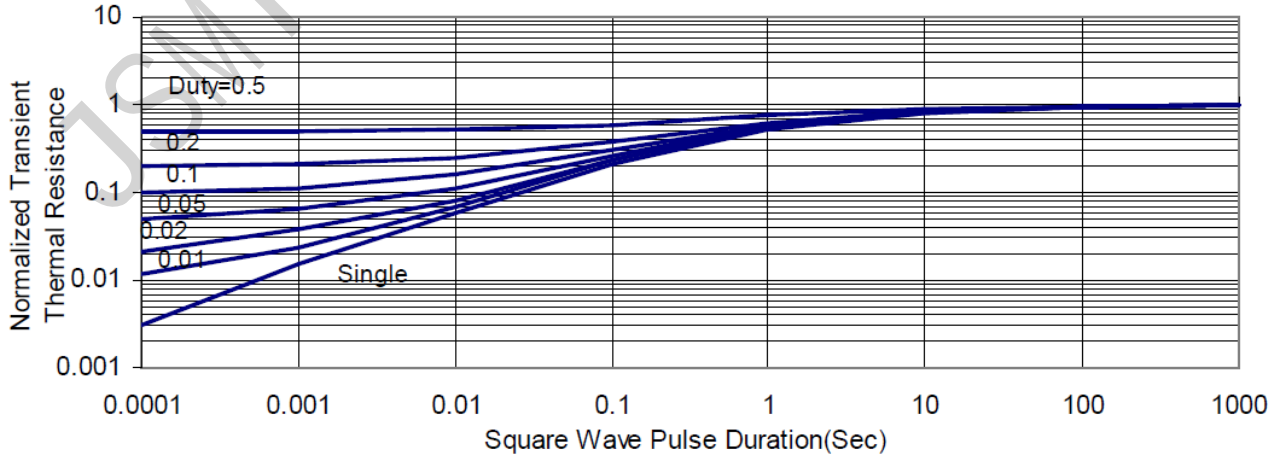
Power Dissipation



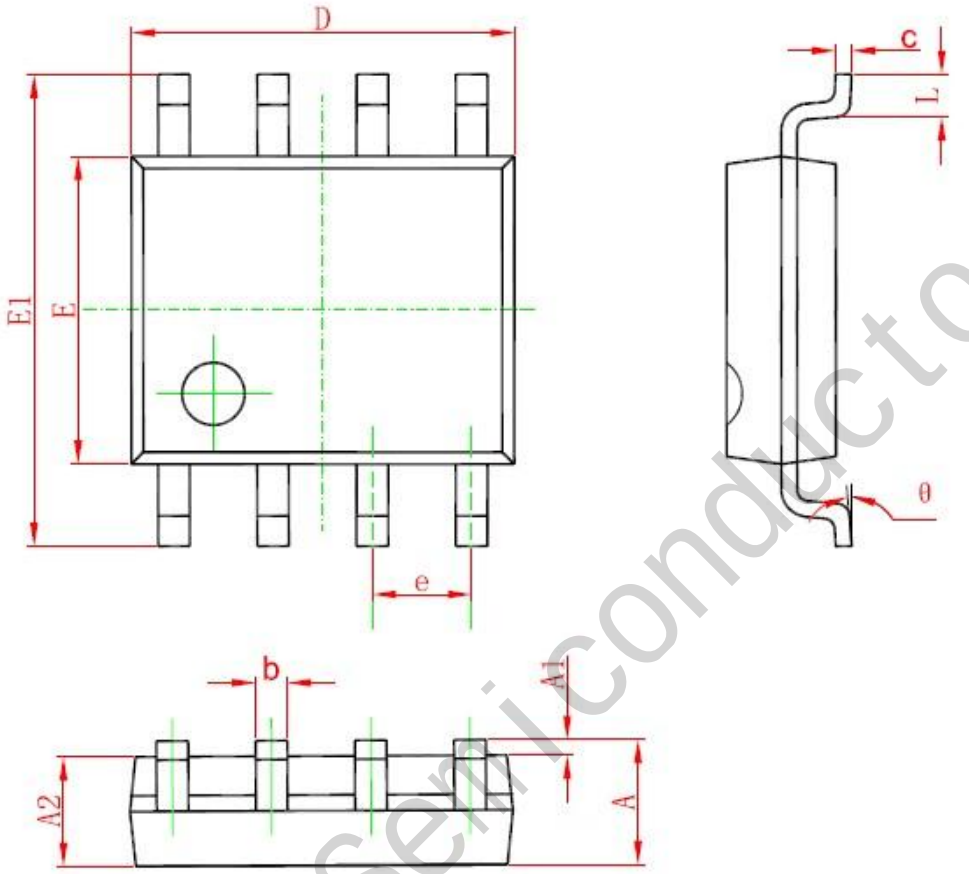
Drain Current



Thermal Transient Impedance



■ *SOP8 PACKAGE OUTLINE DIMENSIONS*



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°